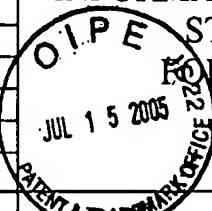


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Serial No.	10/785,310	
Filing Date	February 24, 2004	
Group Art Unit	2818	
Examiner Name	Tu Tu V. Ho	
Allowed	April 28, 2003	
Confirmation No.	9673	
Attorney Docket No.	400.264US01	
Title: 4F2 EEPROM NROM MEMORY ARRAYS WITH VERTICAL DEVICES		

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*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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Serial No.	10/785,310	
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Examiner Name	Tu Tu V. Ho	
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